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DC-link capacitor voltage control for single-phase shunt active power filter with step size error cancellation in self-charging algorithm

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Abstract: This study presents an improved self-charging algorithm by introducing a new feature known as step size error cancellation for better performance of DC-link capacitor voltage control in single-phase shunt active power filter (SAPF). Previous works of self-charging algorithms were focused only for steady-state operation by using either proportional–integral (PI) or fuzzy logic control (FLC). However, in a certain operation of any power system, dynamic operation may also happen. Thus, by introducing step size error cancellation as an additional feature to the self-charging algorithm, both steady state and dynamic operations can be covered. For evaluation and comparison analysis, self-charging with PI and FLC algorithms have been developed too. All the algorithms were simulated in MATLAB–Simulink, respectively, together with the single-phase SAPF. For hardware implementation, the proposed algorithm was programmed in TMS320F28335 digital signal processing board. The other two conventional self-charging algorithms were also programmed for comparison purposes. From the results and analysis, the proposed self-charging with step size error cancellation shows the best performance with high accuracy, fast response time and less overshoot and undershoot. It performs well in both steady state and dynamic operations as compared with both previous self-charging techniques which only work well in steady-state operation.

1 Introduction

Power quality is defined as wide variety of electromagnetic phenomena that characterises the voltage and current at a given time and at a given location in the power system [1]. Possible power problems manifested in voltage, current or frequency deviations, that cause failure or misoperation of customer equipment, are considered as power quality problems [2]. Power quality problems are categorised as transients, voltage variations, harmonics, inter-harmonics, flicker, voltage imbalance and frequency deviation [2, 3]. Harmonics are the main power quality problems in power system which can be mitigated by using active power filter (APF). Harmonics can be categorised into voltage and current harmonics. Current harmonics are caused by nonlinear load operations produced by power electronic devices and applications injected into the supply network through point of common coupling [4]. The major drawbacks of current harmonics are capacitor blowing, equipment overheating, motor vibration and excessive neutral currents [5]. To mitigate the current harmonics, shunt active power filter (SAPF) is used rather than series APF which mitigates voltage harmonics.

In SAPF, opposite direction of harmonic current is injected to the power system to ensure sinusoidal shape at the fundamental frequency of the source current. Established topology for single-phase SAPF is by using full-bridge inverter where it consists of four switching devices and a capacitor named as DC-link capacitor. The main function of DC-link capacitor is to act as a constant DC storage for the inverter to produce the injection current (mitigation current) to the source current. The conventional method to control the DC-link capacitor voltage is by using direct change between instantaneous voltage and desired DC-link voltage. However, by using this method, the DC-link capacitor voltage is not accurately controlled and regulated, and as a result, unclean voltage is produced [6–14]. This major disadvantage contributes to numerous effects such as capacitor blowing and high total harmonic distortion (THD) due to unstable injection current [6].

In recent years, self-charging algorithm has received special attention from the researchers due to its advantages as compared with the conventional algorithm of DC-link capacitor voltage control [15–20]. Among its advantages are it gives high accuracy DC voltage and produces clean regulated voltage with almost no noise, spikes and ripples. The self-charging algorithm uses energy conversion law to control the charging and discharging of the DC-link capacitor as compared with the conventional algorithm which only assumes the difference between desired voltage and next charge voltage of the DC-link capacitor as the main parameter for controlling the capacitor voltage.

Proportional–integral (PI) [15–19] and fuzzy logic control (FLC) [20] are among the existing control techniques to control the voltage error produced from the self-charging algorithm. Self-charging with PI algorithm is popular as it is considered simple; however, it has some drawbacks, such as

- Fluctuation and imbalance of the DC-link voltage [7].
- Large overshoot and slow response [9].
- Existing of ripples, noise and spikes in the regulated DC-link voltage [11, 12].
- Unsatisfactory performance under parameter variations, nonlinearity and load disturbances; it only works in steady-state operation [13, 14].

PI is also hard to be tuned and designed especially by involving SAPF, because it needs to have precise mathematical model to obtain the gains for proportional k_p and integral k_i. As an alternative, with high growth of artificial intelligent techniques, FLC as one of them has much better performance, such as much faster, accurate and very stable, and it works well with complex

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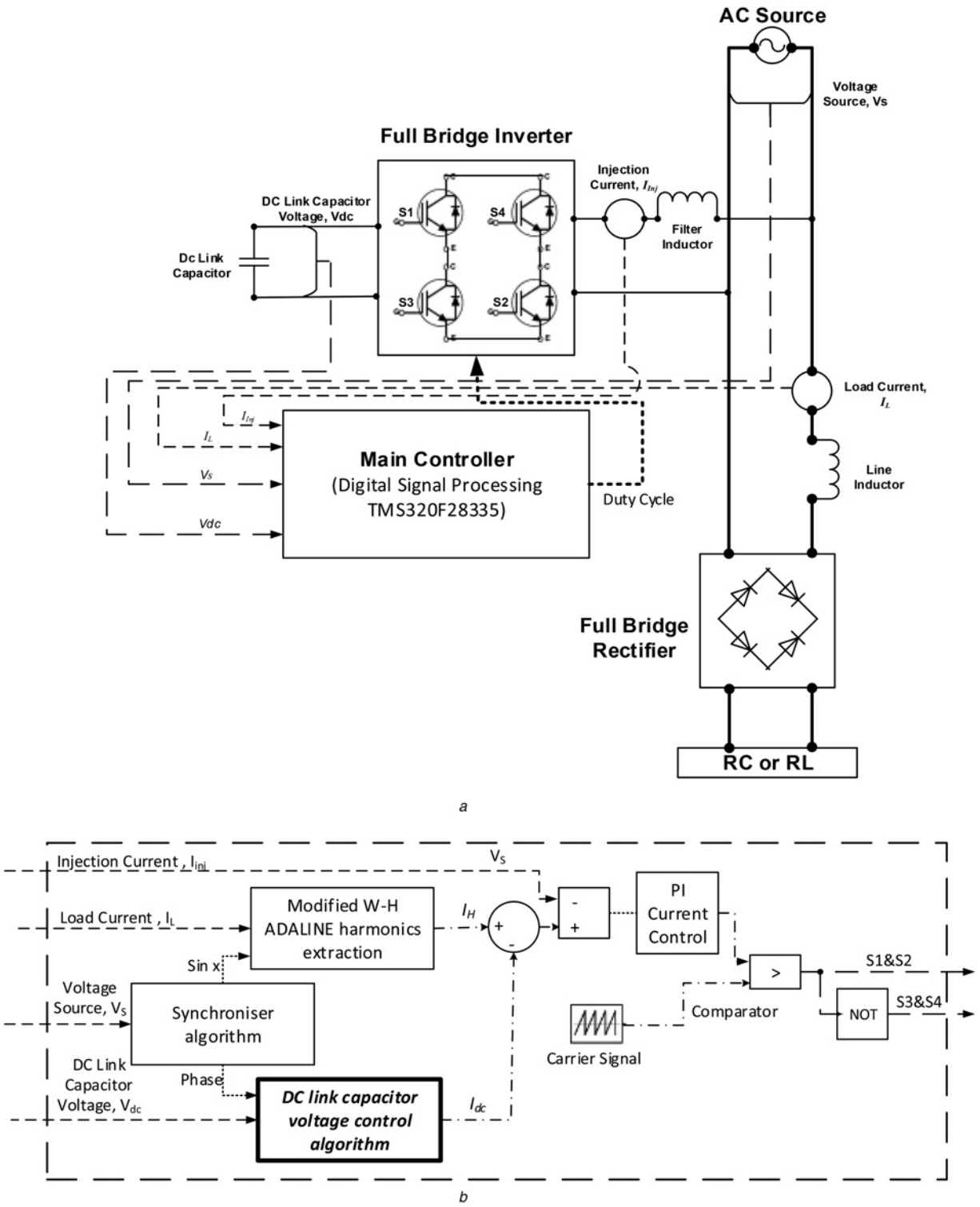

Fig. 1 *Single-phase SAPF*

a Circuit diagram
b Control strategies

system [21–25]. FLC technique does not require specific and precise mathematical models for designing and tuning, and it works well using imprecise inputs, effectively handles non-linearity system and, is more robust and simpler than the PI technique [21–23]. It is also self-acting mechanism and works according to a set of simple and readable linguistic (if–then) rules [24, 25].

Even though FLC technique is much better than PI technique, both of them have same major drawbacks where their operations did not consider parameter variables, nonlinearity and load disturbances; the previous works only considered the steady state operation and no further analysis have been done with dynamic operation [17–20]. Dynamic operation always happens in the power system, and specifically for DC-link capacitor, it may blow when over voltage happens, and possible misoperation of injection current occurs when under voltage happens. Whenever there is a change in the load, the voltage across the DC-link capacitor also undergoes a corresponding change [10]. Specifically for the self-charging algorithm, the existing approach is using PI or FLC to control the

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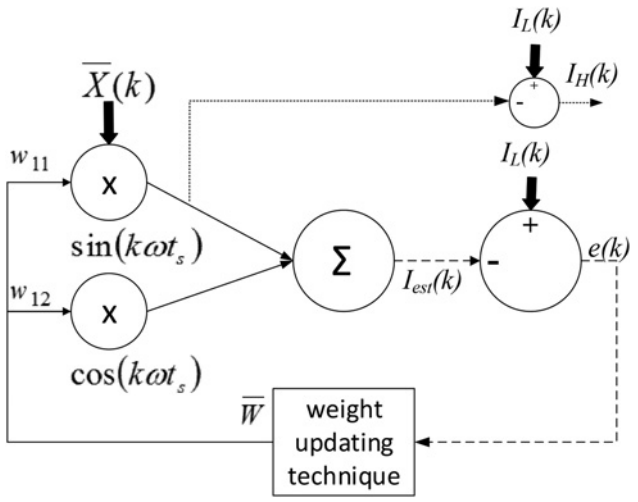

Fig. 2 *Modified W–H ADALINE algorithm [35]*

voltage error directly, thus leads to possible disturbance towards learning response of the algorithm. By controlling the voltage error, which is a direct control approach (main control signal), there is no such flexibility where either the voltage error changes or not, it still has to be processed and controlled.

Therefore, this paper presents a work on improving self-charging algorithm which should be able to increase performance by controlling the DC-link capacitor in steady state and dynamic operations. By introducing additional feature known as the step size error cancellation into the self-charging algorithm, it should be able to handle steady state and dynamic operations. The proposed self-charging algorithm is evaluated and compared with both existing self-charging with PI and FLC algorithms. To further explain about this work, Section 2 in this paper covers the proposed single-phase SAPF, Section 3 covers the harmonics extraction used in the SAPF and followed by discussion on self-charging algorithm with PI and FLC, and further improvements made to it in Section 4. Simulation work and hardware implementation including the results are discussed in Sections 5 and 6, respectively. Finally, Section 7 concludes findings from this work.

2 Single-phase SAPF

Fig. 1 shows the overall SAPF which contains full bridge inverter, DC-link capacitor and controller. The source of harmonics is from rectifier-based circuit which produces one of the highest harmonics in electrical system [26–28]. It is connected with two types of non-linear loads: inductive and capacitive. The SAPF's control strategies consist of harmonics extraction algorithm, DC-link capacitor voltage control algorithm, synchroniser, current control algorithm and switching algorithm. In this paper, the highlighted algorithm is the DC-link capacitor voltage control algorithm. For harmonics extraction, modified Widrow–Hoff (W–H) ADALINE algorithm is used [29–35]; meanwhile, for current control algorithm, PI technique is used [29, 30, 34]. A synchroniser is used to produce reference sinusoidal signal, and meanwhile, pulse-width modulation technique is used for switching algorithm. As mentioned in the introduction, DC-link capacitor voltage control is one of the main control strategies in SAPF. A good DC-link capacitor voltage must be over than two-third of the grid voltage in order to make sure that a proper injection current will be generated. Minimum capacitance value of the capacitor can be

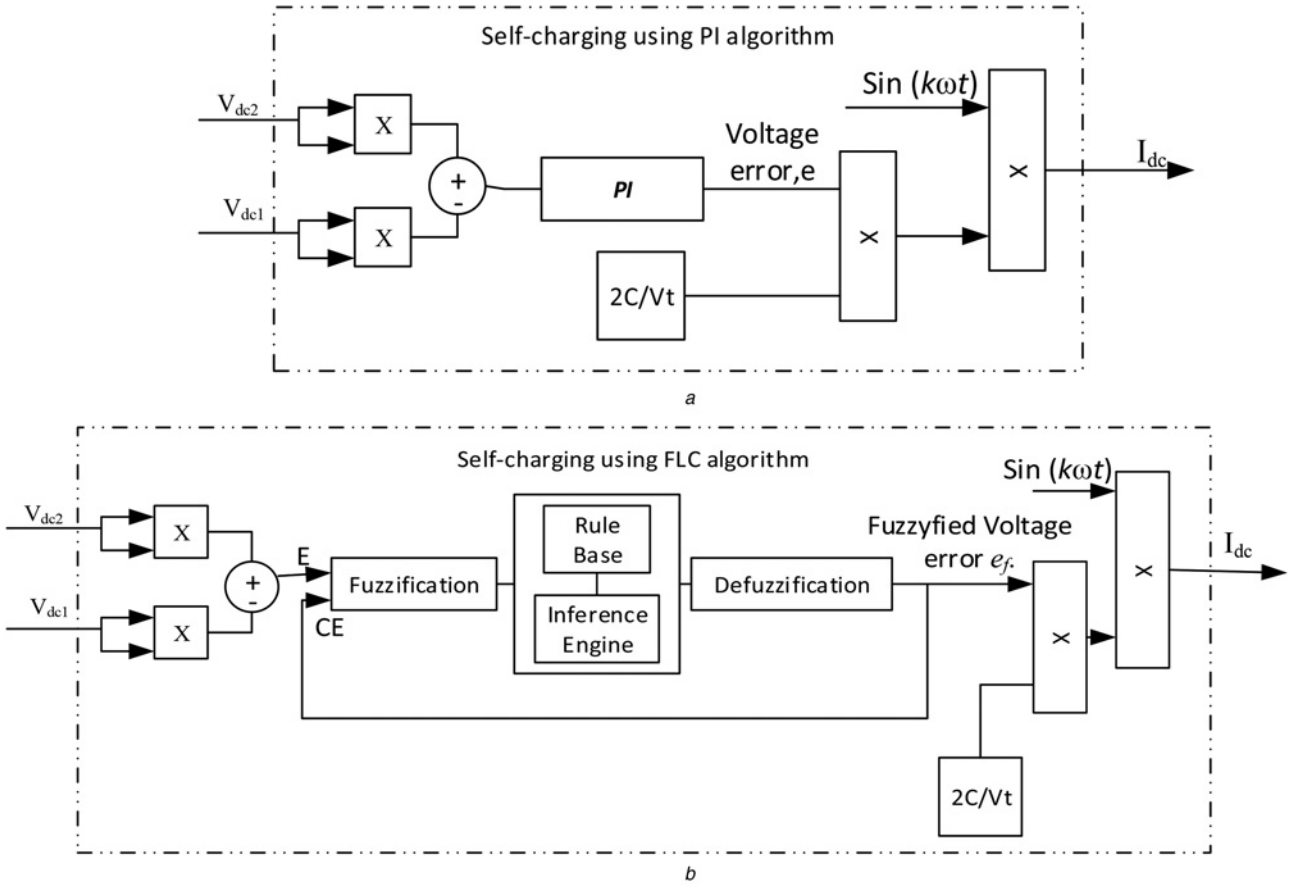

Fig. 3 *Self-charging technique using*
a PI algorithm
b FLC algorithm

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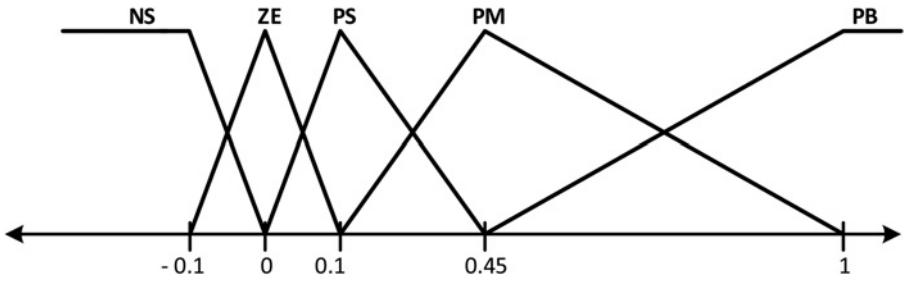

Fig. 4 *Membership functions for E, CE and e_f [20]*

determined as below [36, 37]

$$C \geq \frac{\max\left|\int_0^t I_{\text{inj}}(t)\right|}{\Delta V_{C\max}} \tag{1}$$

where I_{inj} represents the injection current and $\Delta V_{C\max}$ represents the maximum ripple voltage of the DC-link capacitor.

3 Harmonics extraction

Harmonics extraction using ADALINE algorithm performs by using the principle of sine and cosine components (periodic signal) based on the concept of estimating harmonic components that exist in the electrical system. Fundamental component and harmonic components are represented by the non-linear load current I_{L} for each sample k and sample period t_{s} in digital operation with assigned fundamental frequency ω [29–35]. The non-linear load current can be represented as below

$$I_{\text{L}}(k) = \sum_{n=1,2\ldots}^{N} \left[W_{an}\sin\left(nk\omega t_{\text{s}}\right) - W_{bn}\cos\left(nk\omega t_{\text{s}}\right)\right] \tag{2}$$

where W_{an} and W_{bn} are amplitudes of the sine and cosine components of the load current, n is the order of the harmonic to N maximum order. Equation (2) can be arranged to vector form as follows

$$\overline{I}_{\text{L}}(k) = \overline{\boldsymbol{W}}^{\text{T}}\overline{X}(k) \tag{3}$$

where the weight matrix is $\overline{\boldsymbol{W}}^{\text{T}} = \left[w_{11}w_{21}, \ldots, w_{an}w_{bn}\right]$ and $\overline{\boldsymbol{X}}$ represents the sine and cosine vector as

$$\overline{\boldsymbol{X}} = \begin{bmatrix} \sin\left(k\omega t_{\text{s}}\right) \\ \cos\left(k\omega t_{\text{s}}\right) \\ . \\ . \\ \sin\left(nk\omega t_{\text{s}}\right) \\ \cos\left(nk\omega t_{\text{s}}\right) \end{bmatrix}$$

The algorithm is used to train equivalent value of $I_{\text{L}}(k)$. The main feature of this extraction algorithm is the weights updating technique where the W–H method is used [29–35]. Injection current I_{inj} is used to compensate harmonic distortion, which is direct opposite polarity to harmonic current I_{H}, as shown in Fig. 2.

Table 1 Rule-base for self-charging with FLC algorithm [20]

CE\E	NS	ZE	PS	PM	PB
NS	NS	NS	ZE	PS	PM
ZE	NS	ZE	PS	PM	PB
PS	ZE	PS	PM	PB	PB

One of the improvements made in modified W–H ADALINE is it uses only the first order of harmonic components rather than n number of harmonic components as in normal W–H ADALINE.

By using this algorithm, it has overcome problem of the conventional W–H ADALINE algorithm where number of weights n must be updated which requires longer response time [35]. It needs only to update the two weights of the fundamental component, making it is independent of number of harmonic orders. This improvement is based on the mathematical relationship of the elements being orthogonal to each other. With this modification, the iteration speed is greatly enhanced, resulting in faster estimation. However, updating only the two weights results in a large average square error e, and thus learning rate α must be added as in (4) [35]

$$\overline{W}(k+1) = \overline{W}(k) + \frac{\alpha e(k)\overline{Y}(k)}{\overline{Y}^{\text{T}}(k)\overline{Y}(k)} \tag{4}$$

where

$$\overline{W} = \begin{bmatrix} w_{11} \\ w_{21} \end{bmatrix}, \quad \overline{Y} = \begin{bmatrix} \sin\left(k\omega t_{\text{s}}\right) \\ \cos\left(k\omega t_{\text{s}}\right) \end{bmatrix}$$

and α is learning rate. Suitable learning rate is important as it will help the algorithm to optimally produce the accurate fundamental of harmonic current. The harmonic current $I_{\text{H}}(k)$ can be produced from load current deduction (from load current's fundamental sine part) as in (5) [30]

$$I_{\text{H}}(k) = I_{\text{L}}(k) - W\sin\left(k\omega t_{\text{s}}\right) \tag{5}$$

4 DC-link capacitor voltage control

4.1 Self-charging with PI and FLC algorithms

An additional real power has to be drawn to regulate the DC-link capacitor voltage from the supply side or the grid to charge the capacitor. During the charging process, voltage of the DC-link capacitor always changes from the desired voltage which contributes to difference in energy stored in the DC-link capacitor itself. Therefore, the difference in energy stored ΔE in the DC-link capacitor is represented as below

$$\Delta E = \frac{C}{2}\left[\left(V_{\text{dc2}}\right)^2 - \left(V_{\text{dc1}}\right)^2\right] \tag{6}$$

where C is the capacitance value of the DC-link capacitor, V_{dc1} is the desired voltage of the DC-link capacitor and V_{dc2} is the instantaneous voltage of the DC-link capacitor. On the other hand, the charging energy delivered by single-phase AC system E_{ac} for the capacitor is

$$\begin{aligned} E_{\text{ac}} &= Pt_{\text{c}} \\ E_{\text{ac}} &= V_{\text{rms}}I_{\text{dc,rms}}\cos\theta t_{\text{c}} \end{aligned} \tag{7}$$

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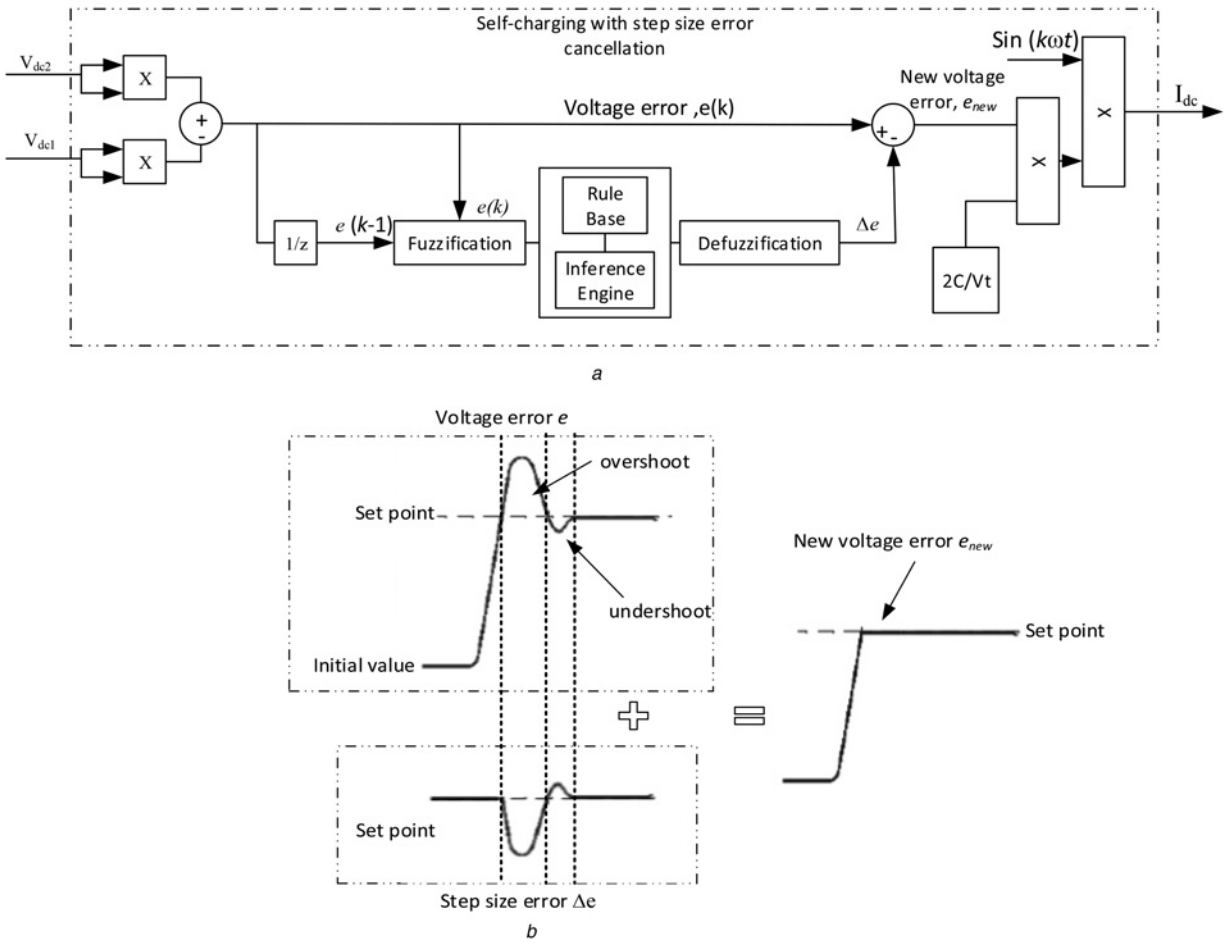

Fig. 5 *Self-charging with step size error cancellation*

a Block diagram
b Conceptual operation

Table 2 Rule-base for self-charging with step size error cancellation

$e\backslash e(k-1)$	NS	ZE	PS	PM	PB
NB	ZE	NS	NB	NB	NB
NS	PS	ZE	NS	NB	NB
ZE	PB	PS	ZE	NS	NB
PS	PB	PB	PS	ZE	NS
PB	PB	PB	PB	PS	ZE

where P is the additional real power required, t_c is the charging time of the capacitor, V_{rms} is the rms value of the supply voltage, $I_{dc,rms}$ is the rms value of the charging capacitor current I_{dc} and θ is the difference of phase angle between supply voltage and charging capacitor current. However, t_c can be defined as $T/2$ since the charging process only takes half of a cycle for the capacitor, where T is the period of the supply frequency, which is 50 Hz. V_{rms} and $I_{dc,rms}$ can be expressed in peak values as below

$$\therefore E_{ac} = \frac{V}{\sqrt{2}}\frac{I_{dc}}{\sqrt{2}}\frac{T}{2}$$
$$E_{ac} = \frac{VI_{dc}T}{4} \tag{8}$$

By neglecting the switching losses in the inverter and according to the energy conservation law, the following equation holds:

$$\Delta E = E_{ac}$$
$$\frac{C}{2}\left[(V_{dc2})^2 - (V_{dc1})^2\right] = \frac{VI_{dc}T}{4} \tag{9}$$
$$\therefore I_{dc} = \frac{2C\left[(V_{dc2})^2 - (V_{dc1})^2\right]}{VT}$$

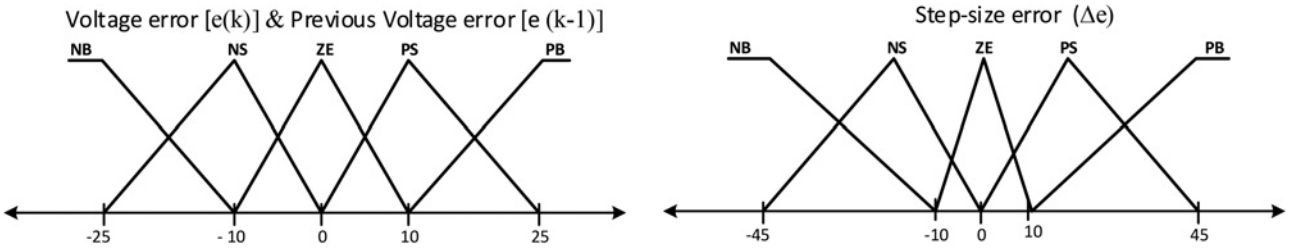

Fig. 6 *Membership functions for the change of voltage error, previous voltage error and step size error*

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Table 3 Parameters and components for SAPF

Type	Value
voltage source, ac	230 V
DC-link capacitor	4700 μF, 400 V
injection inductor	5 mH
line inductor	1 mH
sampling frequency	25 kHz

Table 4 Parameters and setting values for each self-charging algorithm

Parameter	Self-charging with PI algorithm	Self-charging with FLC algorithm	Self-charging with step size error cancellation
K_p	21		
K_i	7		
number of membership functions		3	3
number of rules		15	25

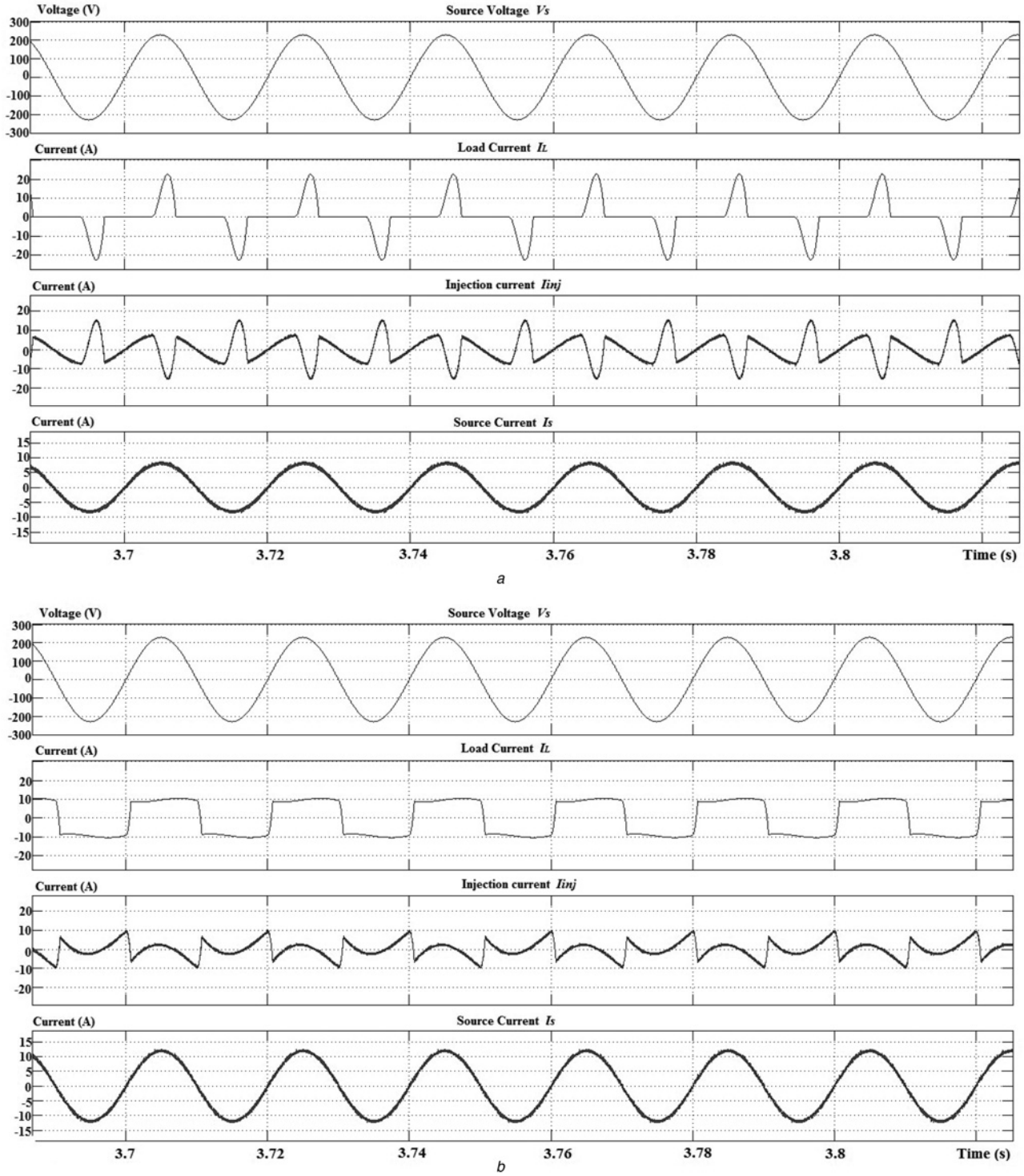

Fig. 7 *Simulation result of SAPF which covers source voltage V_s, load current I_L, injection current I_{inj} and source current I_s, for*

a Inductive load
b Capacitive load

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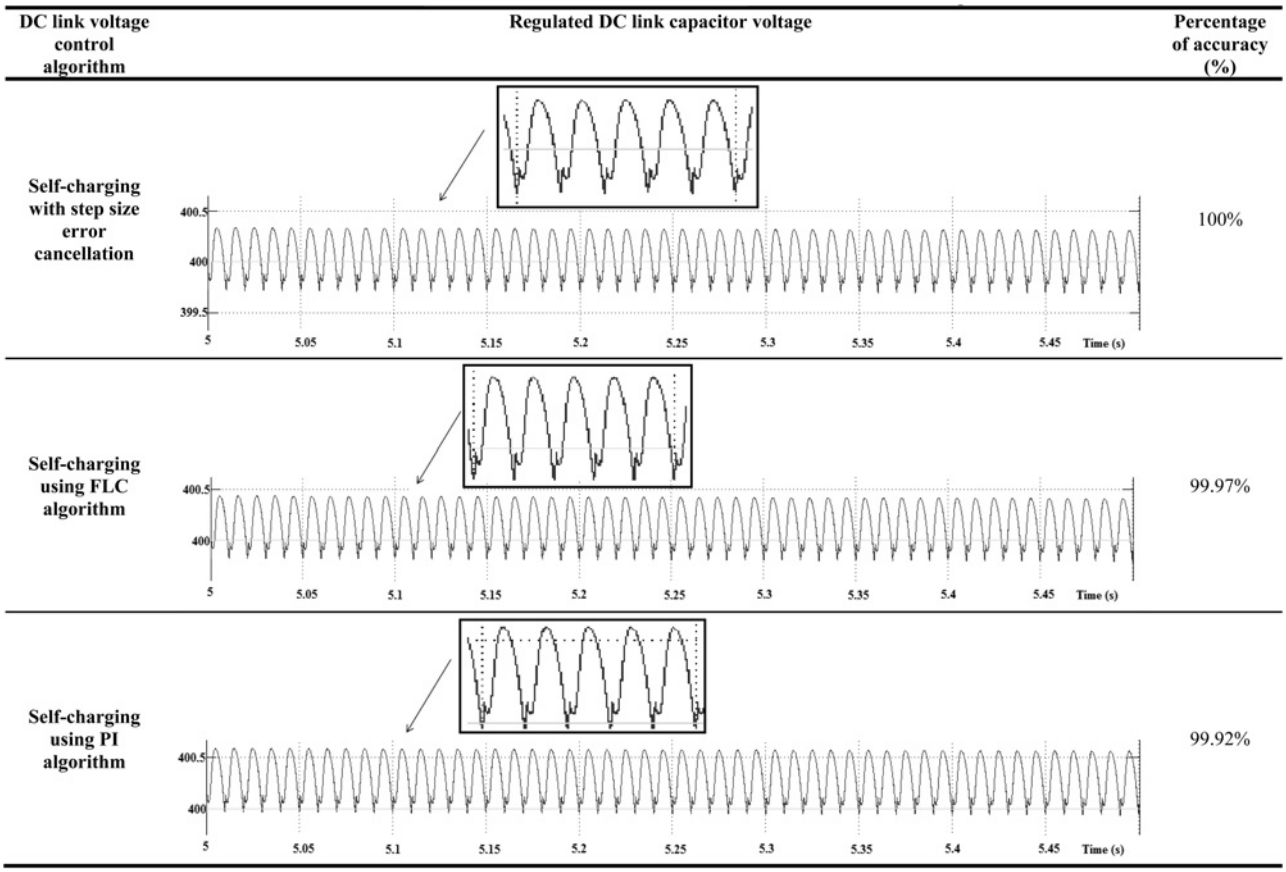

Fig. 8 *Performance of DC-link voltage control algorithms for inductive load with the desired voltage of 400 V*

Voltage error e is defined as

$$e = \left(V_{\mathrm{dc2}}\right)^2 - \left(V_{\mathrm{dc1}}\right)^2 \tag{10}$$

The voltage error e in the self-charging algorithm gives the highest effect towards determination of DC-link capacitor charging current I_{dc}. The DC-link capacitor voltage algorithm is desired to control the recharge rate by regulating the I_{dc} (refer to Fig. 1*b*). As mentioned in the introduction, PI was widely utilised in DC-link capacitor voltage control. Fig. 3*a* shows block diagram of self-charging with PI algorithm. The minimum values of parameters for PI technique can determined as below [11]

$$k_{\mathrm{p}} \geq 2C\xi\omega \tag{11}$$

$$k_{\mathrm{i}} \geq C\omega \tag{12}$$

where k_{i} represents integral gain, k_{p} represents proportional gain, C represents the capacitance value of the DC-link capacitor, ξ represents damping factor which is usually 0.707 and ω represents the angular frequency.

The self-charging with FLC algorithm is shown in Fig. 3*b*. FLC is divided into four categories, which include fuzzification, fuzzy inference, rule-base and defuzzification. During fuzzification, the numerical input variables are converted into linguistic variables based on the membership functions. Various fuzzy levels could be used for input and output variables. The self-charging with FLC algorithm uses error E and change in error CE as inputs with sample time k, as shown in (13) and (14); while the output of FLC algorithm is the fuzzyfied voltage error e_{f}.

$$E(k) = \left(V_{\mathrm{dc2}}\right)^2 - \left(V_{\mathrm{dc1}}\right)^2 \tag{13}$$

$$CE(k) = e_{\mathrm{f}}(k) \tag{14}$$

After E and CE are obtained, these inputs are converted into linguistic variables and then the fuzzy output is generated by looking up in a rule-base table. The FLC algorithm is based on master rule of 'If X and Y, Then Z'. To determine the output of the fuzzy logic, the fuzzy inference is used. The method for inference is Mamdani [38]. Usually, weights are added to the rules to improve reasoning accuracy and to reduce undesirable consequent. The fuzzy output is converted back to numerical variable from linguistic variable during defuzzification. The most common method used for this defuzzification is the centroid of area since it has good averaging properties and more accurate results can be produced [39]. The membership functions in the self-charging with FLC algorithm are shown in Fig. 4 and the rule-base is shown in Table 1.

4.2 Self-charging with step size error cancellation

In order to address dynamic operation, an improvement to the self-charging algorithm is carried out by introducing step size error cancellation as shown below

$$\begin{aligned} e_{\mathrm{new}} &= e + \Delta e \\ e_{\mathrm{new}} &= \left[\left(V_{\mathrm{dc2}}\right)^2 - \left(V_{\mathrm{dc1}}\right)^2\right] + \Delta e \end{aligned} \tag{15}$$

where e_{new} is the new voltage error, e is the voltage error as in (10) and Δe is the proposed step size error. Thus, the new charging current I_{dc} is

$$\therefore I_{\mathrm{dc}} = \frac{2C\left[\left[\left(V_{\mathrm{dc2}}\right)^2 - \left(V_{\mathrm{dc1}}\right)^2\right] + \Delta e\right]}{VT} \tag{16}$$

When the capacitor voltage is controlled at desired set point, the

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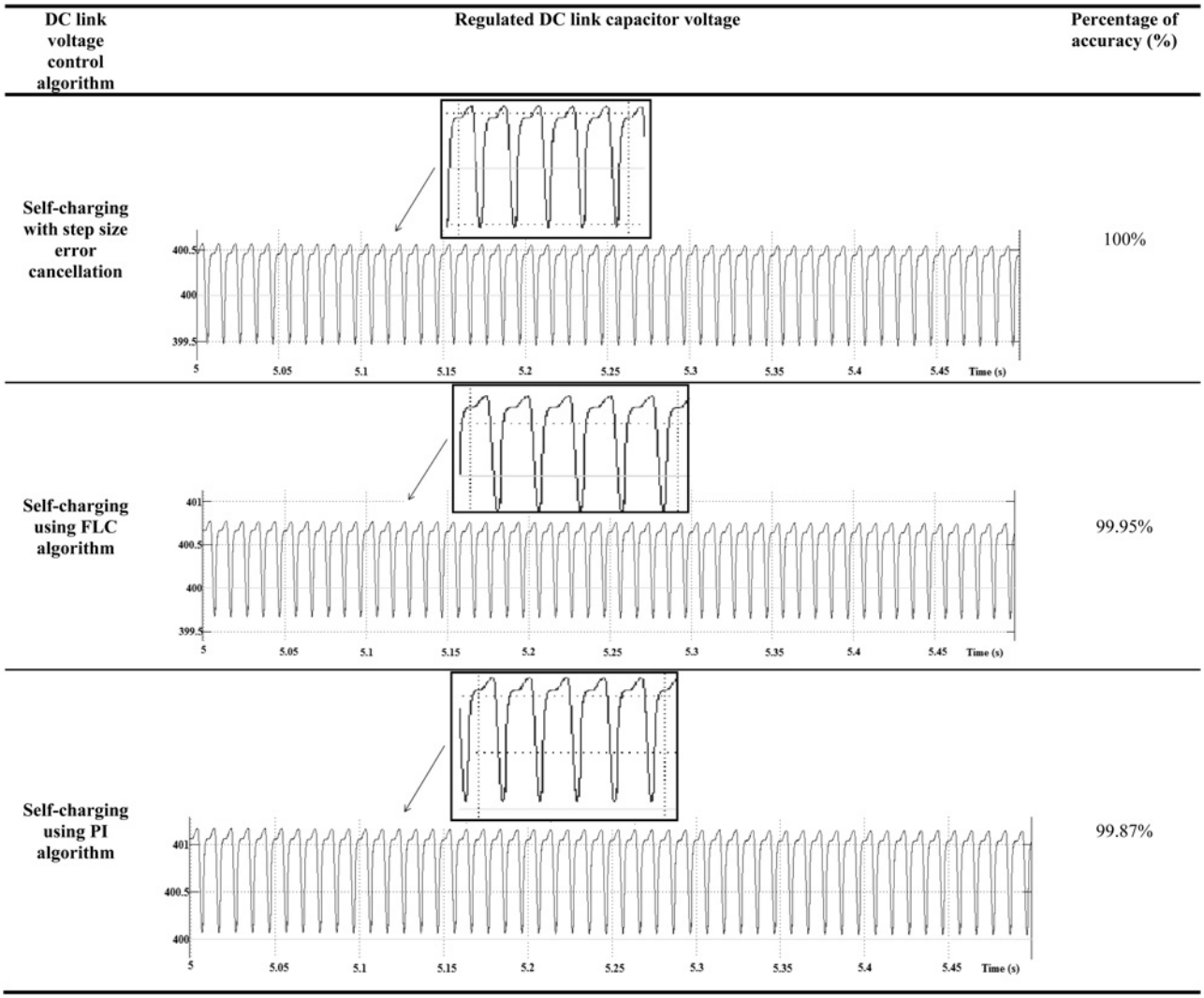

Fig. 9 *Performance of DC-link voltage control algorithms for capacitive load with the desired voltage of 400 V*

charging DC-link capacitor current I_{dc} must be or almost equals to zero. Rather than directly control the voltage error, step size error cancellation is added in the self-charging algorithm as shown in Fig. 5*a*. Its main function is to give flexibility for the algorithm to cancel any change of voltage error in terms of overshoot and undershoot. There will be no disturbance occurs directly since the self-charging with step size error cancellation algorithm provides alternative path to control the voltage error, rather than the self-charging with PI and FLC algorithms which directly control the voltage error. This modification contributes to fast response and improved performance. If any overshoot or undershoot happens to the voltage error, the improved self-charging will cancel all overshoot and undershoot and directly make them equal to zero. If overshoot happens, then Δe will be negative, and meanwhile, when undershoot happens, Δe will be positive; both to counter back the overshoot and undershoot of the voltage error. The step size error will only give effect towards the equation if any overshoot or undershoot happens to the voltage error especially after the capacitor voltage reaches the desired voltage.

To control Δe, FLC technique is chosen as its strong advantages over PI technique are clearly mentioned earlier. FLC is used to control the step size because the cancellation must be precise and accurate to obtain the desired results. Some modifications have been made to optimise the FLC technique, which involve fuzzification inputs and number of fuzzy rules. Existing self-charging with FLC algorithm uses E and CE as the main inputs for fuzzification, but for the self-charging with step size error cancellation, the fuzzification inputs are set to voltage error $e(k)$ and previous voltage error $e(k-1)$. Fig. 6 shows the membership functions of the FLC technique and Table 2 shows the rule-base; both for the self-charging with step size error cancellation. The mappings of the membership functions are created based on open-loop real data of the voltage error e.

5 Simulation results

The proposed single-phase SAPF was connected to the test bed which consists of supply grid source and non-linear loads. Two types of non-linear loads were developed by using a diode H-bridge rectifier with 470 μF capacitor and 50 Ω resistor (capacitive) connected in parallel as the first one, and meanwhile 160 mH inductor and 15 Ω resistor (inductive) connected in series for the second one. Simulation works were carried out under steady state and dynamic operations using the self-charging with step size error cancellation as the proposed DC-link capacitor voltage control. In addition, for comparison purpose, the self-charging with PI algorithm and the self-charging with FLC algorithm were used too. The sampling time for simulation was set to 150 μs. Table 3 shows parameters and components for single-phase SAPF, and meanwhile, Table 4 provides the significant parameters with their setting values used in these three self-charging algorithms.

The main important factors used to analyse performance for each DC-link capacitor voltage control algorithm are percentage of accuracy, overshoot, undershoot and response time. The percentage of accuracy PA is referred to the ratio of the average

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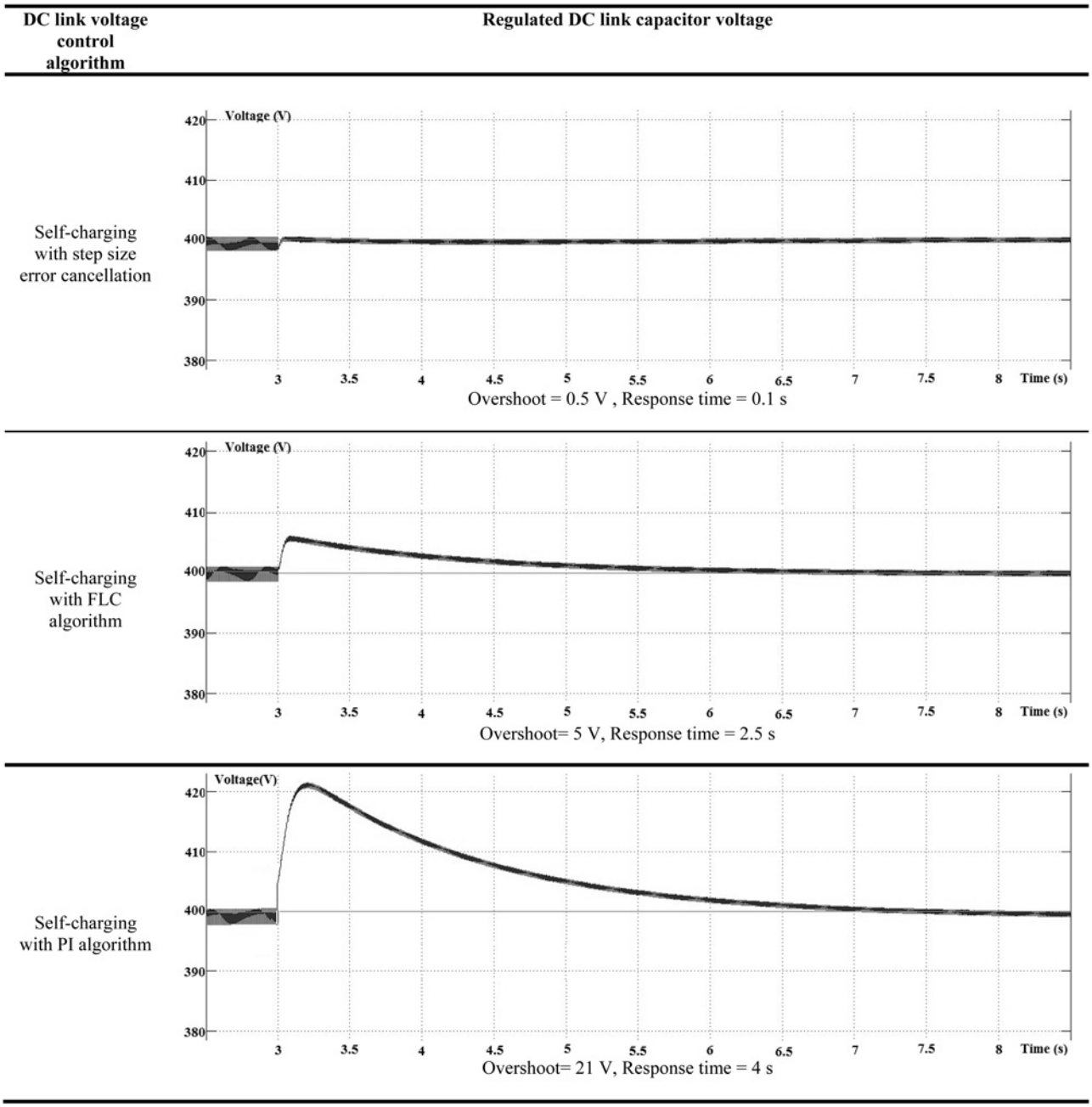

Fig. 10 *Performance of DC-link voltage control algorithm for capacitive to inductive*

output of DC-link capacitor voltage $V_{dc,average}$ with the desired DC-link capacitor voltage $V_{dc,desired}$, as shown below

$$\therefore PA = \frac{V_{dc,average}}{V_{dc,desired}} \times 100 \tag{17}$$

For performances in related to response time, overshoot and undershoot, dynamic operations through load change tests were done when the changes were performed from capacitive to inductive and from inductive to capacitive, respectively. Fig. 7 shows the simulation result of SAPF which covers source voltage V_s, load current I_L, injection current I_{inj} and source current I_s, for both inductive and capacitive loads. From Fig. 7, the source current I_s is properly compensated and the harmonics are removed which resulting THDs of 2% for the inductive load and 3.13% for the capacitive load; both are below 5%, as to follow IEEE Standard 519-2014: IEEE Recommended Practices and Requirements for Harmonic Control in Electric Power Systems [1].

5.1 Steady-state operation

Performances of each DC-link capacitor voltage control algorithm for inductive and capacitive loads are shown in Figs. 8 and 9, respectively. All self-charging algorithms regulate the DC-link capacitor voltage well, but their percentages of accuracy are different. Among them, the proposed algorithm produces 100% accuracy of the regulated DC-link capacitor voltage for both non-linear loads. The self-charging with FLC algorithm meanwhile produces little bit higher regulated voltages with 0.1 V (99.97% accuracy) and 0.2 V (99.95% accuracy) above the desired voltage for inductive and capacitive loads, respectively. Meanwhile, the self-charging with PI algorithm shows the worst regulated voltages by producing 0.3 V (99.92% accuracy) and 0.5 V (99.87% accuracy) above the desired voltage for inductive and capacitive loads, respectively. From the simulation in steady-state operation, all the self-charging algorithms perform with high accuracy of DC-link capacitor voltage; however, among them, the proposed self-charging algorithm shows the highest accuracy which is about 0.3–0.13% better than the existing self-charging algorithms.

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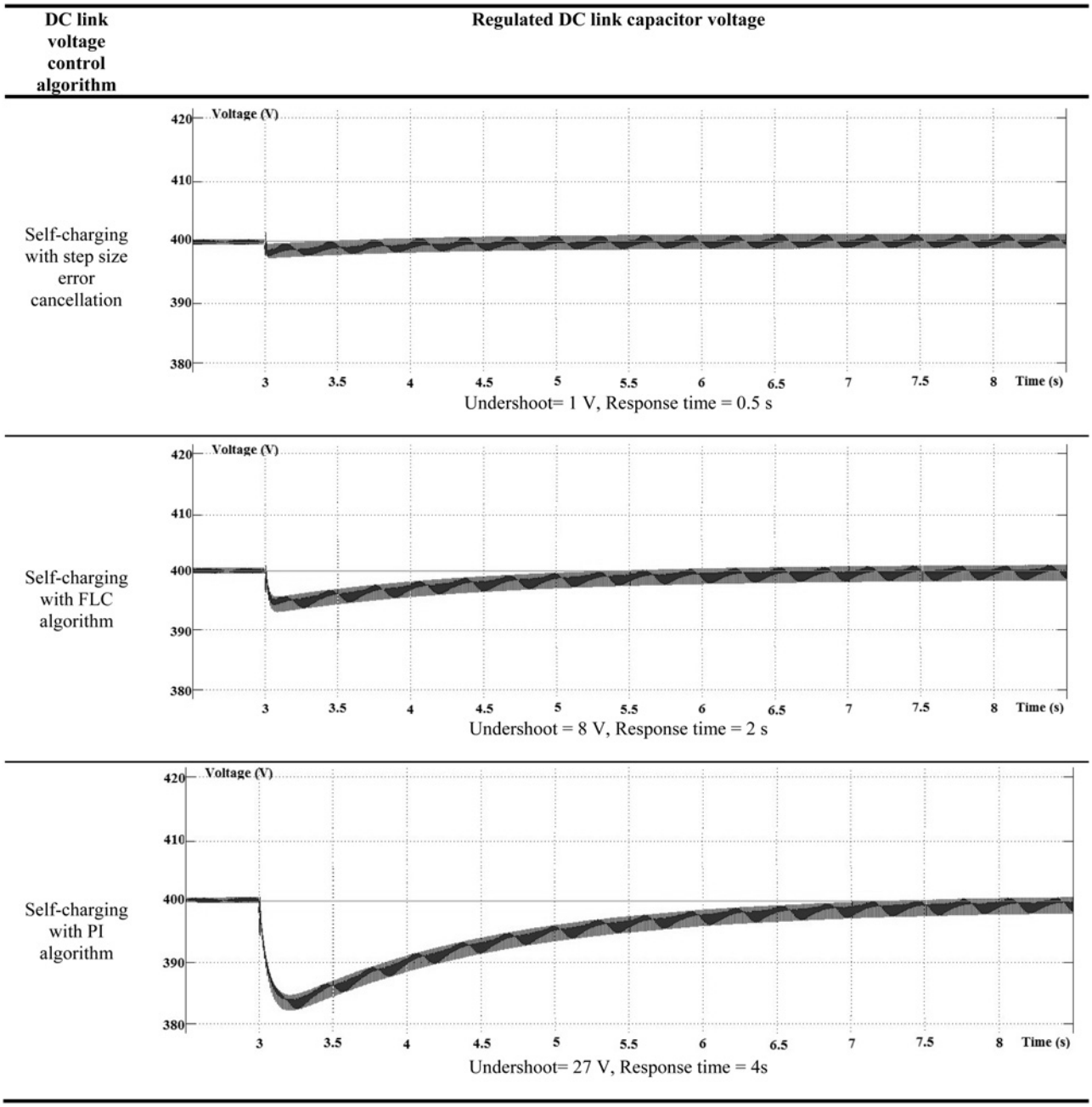

Fig. 11 *Performance of DC-link voltage control algorithm for inductive to capacitive*

5.2 Dynamic operation

Figs. 10 and 11 show the effect of each DC-link capacitor voltage control algorithm towards the regulated DC voltage for operations from capacitive to inductive and inductive to capacitive, respectively. For capacitive to inductive, the self-charging with step size error cancellation algorithm shows the best performance with only overshoot of 0.5 V and response time of 0.1 s. The second best performance is the self-charging with FLC algorithm which performs with overshoot of 5 V and response time of 2 s. The worst performance is shown by the self-charging with PI algorithm with the highest overshoot of 21 V and the longest response time of 4 s. For inductive to capacitive, the self-charging with step size error cancellation algorithm also shows the best performance with undershoot of 1 V and only response time of 0.5 s. On the other hand, the self-charging with PI algorithm shows the worst performance with undershoot of 27 V and response time in about 4 s. The self-charging with FLC algorithm, although is better than the self-charging with PI algorithm, still has high undershoot of 8 V and response time of 2 s.

From all the simulation results, in both steady state and dynamic operations, the self-charging with step size error cancellation algorithm shows the best performance with high accuracy, low overshoot, low undershoot and fast response time. The self-charging with PI and FLC algorithms, as widely used before, perform well under steady-state condition. However, during dynamic operation, those self-charging algorithms do not perform well as they are unable to track and control effect from the fast changing of the non-linear loads. Both algorithms are assigned to control the voltage error directly, disregard either the voltage error has certain value or only zero; thus, there is possibility of delay to produce the charging current of the DC-link capacitor due to effect of operation from PI or FLC technique. As a result, they perform with slow tracking which leads to possible high overshoot and undershoot, and slow response time.

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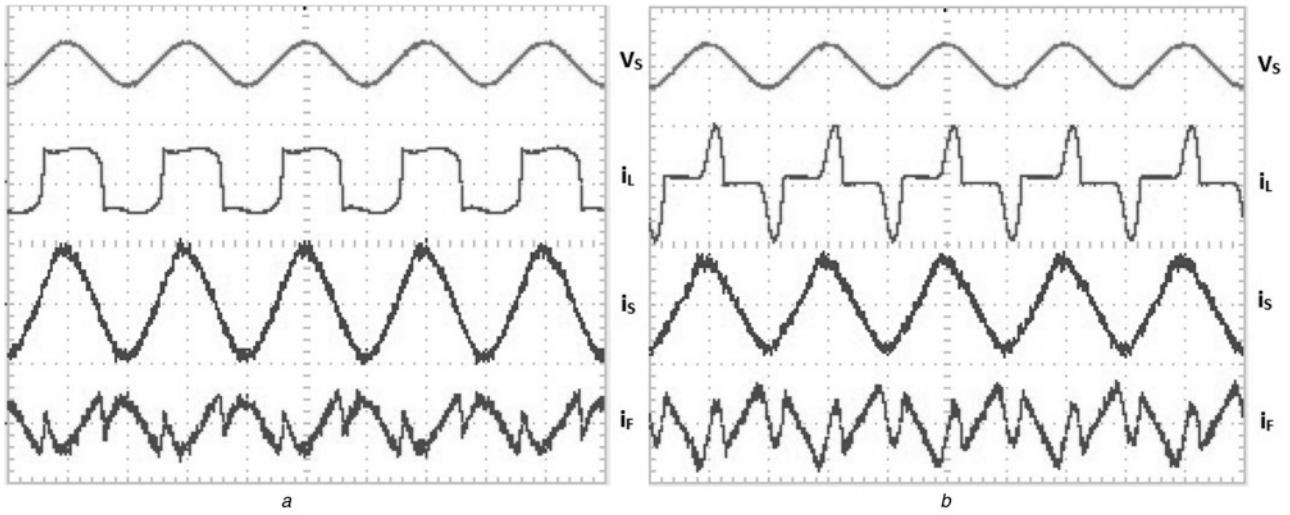

Fig. 12 *Experimental result of SAPF which covers source voltage V_s, load current I_L, injection current I_{inj} and source current I_s, for*

a Inductive load
b Capacitive load

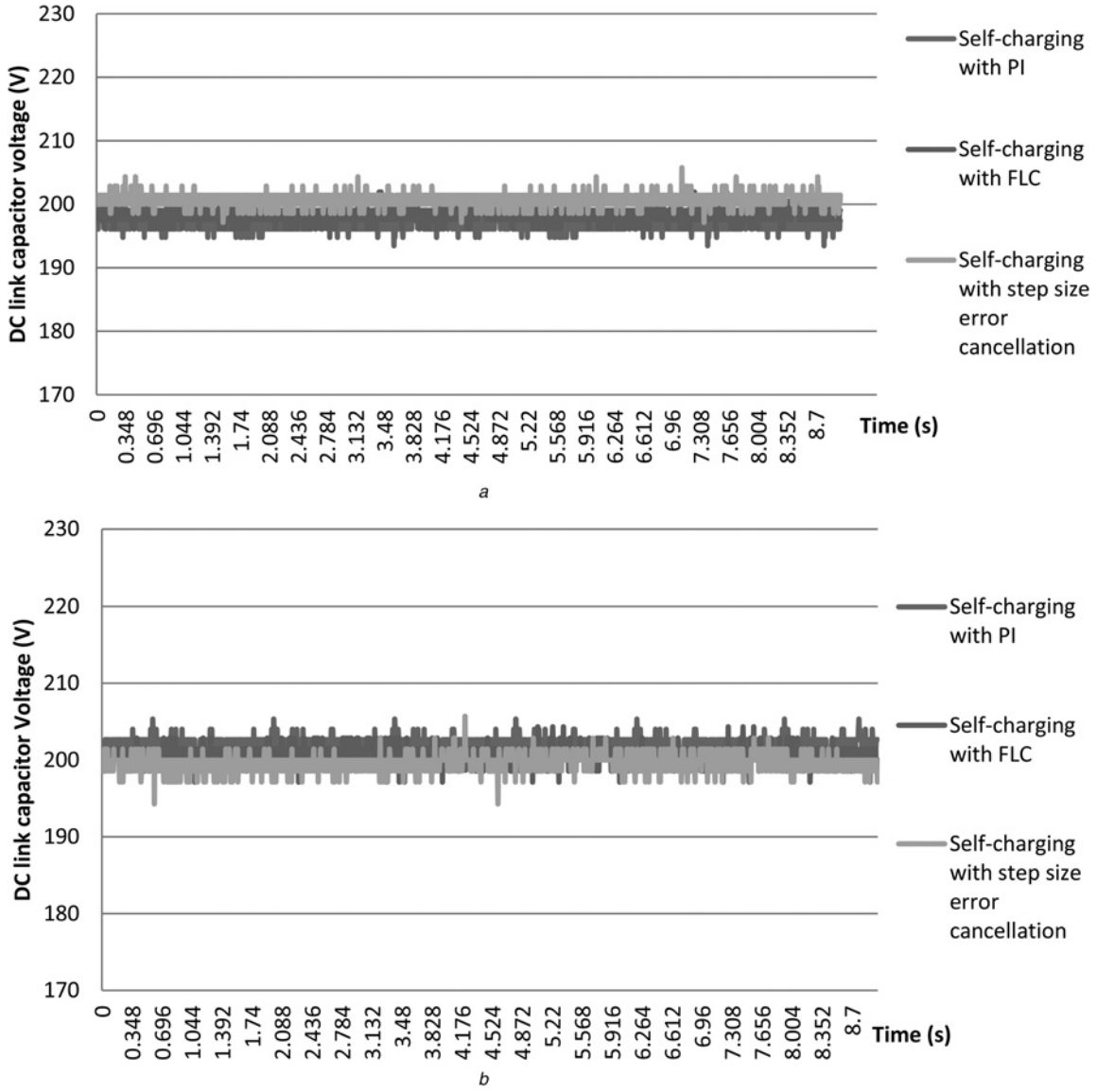

Fig. 13 *Comparison of three DC-link voltage control algorithms in steady-state operation for*

a Inductive load
b Capacitive load

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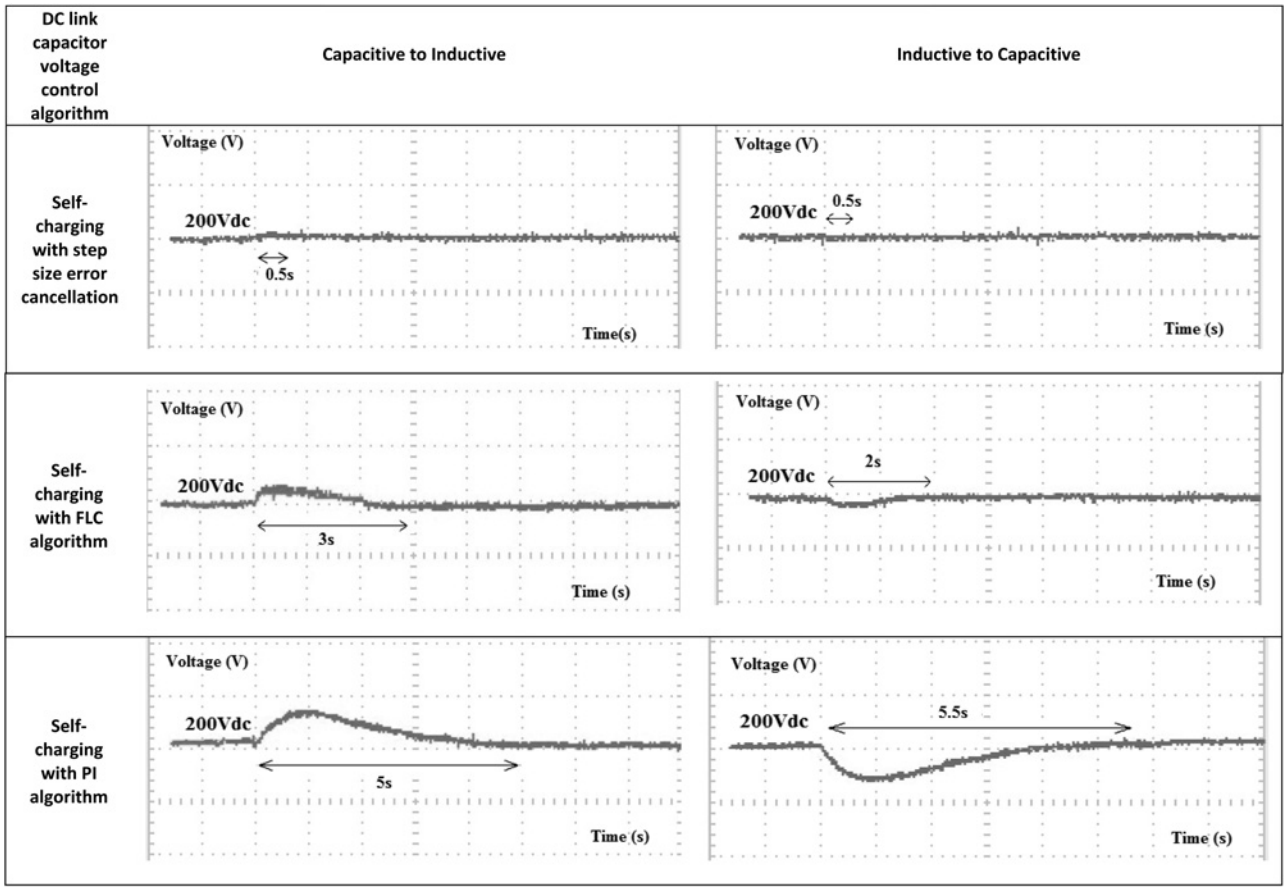

Fig. 14 *Regulated DC-link capacitor voltage in dynamic operation*

6 Hardware implementation

Laboratory prototype has been developed to evaluate practically the proposed algorithm. The single-phase SAPF was constructed as same as already modelled in MATLAB–Simulink. For the testing, the supply source was set to 100 V, which was supplied through variable transformer. Thus, the desired DC-link capacitor voltage was set to 200 V. Digital signal processing TMS320F28335 board was configured and programmed to perform all the control strategies for the single-phase SAPF which include the harmonics extraction, DC-link capacitor voltage control, current control and switching algorithm. The laboratory prototype was also tested under steady state and dynamic operations. Fig. 12 shows the experimental result of SAPF which covers source voltage V_s, load current I_L, injection current I_{inj} and source current I_s, for inductive and capacitive non-linear loads. Fig. 13 shows comparison analysis in steady-state operation between the three DC-link voltage control algorithms for inductive and capacitive loads. Percentages of accuracy obtained from these three algorithms during steady-state operation are summarised as in Table 5. Fig. 14 shows the performance of regulated DC-link capacitor voltage in dynamic operation. Further measurement of overshoot or undershoot, and response time for all these algorithms, is shown in Table 6.

Table 5 Percentage accuracies of all the self-charging algorithms from the experimental work under steady-state operation

DC link voltage control algorithm	Percentage of accuracy, %	
	Inductive	Capacitive
self-charging with step size error cancellation	99.98	99.96
self-charging using FLC algorithm	99.85	99.8
self-charging using PI algorithm	98.9	98.9

By referring to Fig. 13 and Table 5, the self-charging with step size error cancellation shows the highest accuracies for both inductive and capacitive non-linear loads, which are about 99.98 and 99.96%, respectively. The self-charging with FLC algorithm shows the second highest accuracies, which are about 99.85% for inductive load and 99.8% for capacitive load. The worst performance is shown by the self-charging with PI algorithm with the accuracies of 98.9% for both non-linear loads. All three techniques show good accuracy and stability during steady-state operation, but yet, the best performance is shown by the self-charging with step size error cancellation.

For dynamic operation, as can be referred to Fig. 14 and Table 6, for capacitive to inductive, the proposed algorithm shows the lowest overshoot in about 2 V and the fastest response time with 0.5 s. The worst performance is shown by the self-charging with PI algorithm with overshoot of 19 V and response time of 5 s; meanwhile, the self-charging with FLC algorithm shows better performance with

Table 6 Performance of all the self-charging algorithms from experimental work under dynamic operation

DC-link voltage control algorithm	Overshoot or undershoot, V		Response time, s	
	Capacitive to inductive	Inductive to capacitive	Capacitive to inductive	Inductive to capacitive
self-charging with step size error cancellation	2	1	0.5	0.5
self-charging with FLC algorithm	5	5	3	2
self-charging with PI algorithm	19	20	5	5.5

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overshoot of 5 V and response time of 3 s. The same findings observed for inductive to capacitive, where the proposed algorithm shows the lowest undershoot with about 1 V and the response time with only 0.5 s. As expected, the worst performance is shown by the self-charging with PI algorithm with the highest undershoot in about 20 V and the slowest response time of 5.5 s. For the self-charging with FLC algorithm, it shows better performance as compared with the self-charging with PI algorithm with only undershoot of 5 V and response time of 2 s. From both steady state and dynamic operations, the self-charging with step size error cancellation shows the best performance which reveals the significant role of introducing step size error cancellation.

7 Conclusion

This paper has presented a new DC-link capacitor voltage control algorithm which introduces a new feature, known as step size error cancellation. It has been added to enhance the capability of the self-charging algorithm which would indirectly control the voltage error. Indirect control provides flexibility of controlling the voltage error; overcomes the previous algorithms which directly control the voltage error even though there is no such change to its value. As to verify performance of the proposed algorithm, evaluation under both steady state and dynamic operations has been carried out. Analysis in steady-state operation has widely been used before; thus, through additional analysis with dynamic operation which contributes to uniqueness of this work, more comprehensive results and findings have been obtained for further assessment.

The proposed algorithm has successfully been demonstrated and comparative evaluation has been carried out with the established self-charging algorithms with PI or FLC in order to verify its better performance. The simulation work confirms that the proposed algorithm is able to achieve high accuracy in steady-state operation, and low overshoot with fast response time in dynamic operation. Significant different has been observed during dynamic operation where the proposed algorithm is able to control any effect from the changes between the non-linear loads.

Hardware implementation has confirmed effectiveness of the proposed algorithm through both steady state and dynamic operations as carried out in the simulation work. Fast response time, low overshoot and low undershoot clearly show the advantages of the proposed algorithm over the established self-charging algorithms especially during dynamic operation.

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